Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

ME DEGREE END SEMESTER THEORY EXAMINATIONS, NOV /DEC 2024

First Semester

Applied Electronics

PAPT2402 - Advanced Digital System Design

Regulations - 2024

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	What is state assignment and give its significance?	RE	1	2
2.	What are the basic building blocks of ASM chart?	RE	1	2
3.	How do essential hazards affect the circuit?	RE	2	2
4.	What is mean by race round condition?	RE	2	2
5.	What are the limitations of the path sensitization method?	RE	3	2
6.	Outline the types of faults commonly occur in PLAs.	UN	3	2
7.	List the features of FPGA.	RE	4	2
8.	What is the function of the RAM blocks in Xilinx 4000 FPGAs?	RE	4	2
9.	Write the Verilog code for half-adder using gate level modelling?	UN	5	2
10.	Name different type of operators in VHDL code.	RE	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*13 = 65)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a	i	Explain the reduction of state tables and state assignments with examples.	UN	1	7
		ii	Explain the factors influencing the modelling of clocked synchronous sequential circuits.	UN	1	6
			Or			
	b	i	Explain the use of ASM charts in the design of digital circuits with suitable example.	UN	1	7
		ii	Explain the use of HDL in digital system design.	UN	1	6
12.	a		Identify the role of don't care conditions in flow table reduction and how they can be utilized to simplify the design.	AP	2	13
			Or			
	b		Describe the process of creating a state table for a vending machine controller based on its functional requirements.	AP	2	13
13.	a	i	Give the PLA realization of the following functions using a PLA with 5 inputs, 4 outputs and 8 AND gates. F1(a,b,c,d) = ∑m(0,1,2,311,12,13,14,15,16,17,18,19,27,28,29,30,31) F2(a,b,c,d) = ∑m(4,5,6,7,8,9,10,11,20,21,22,23,30)	AN	3	8
		ii	Compare and contrast the stuck at faults and bridge faults.	AN	3	5
			Or			

	b	i	Analyze the procedure involved in D- Algorithm with an example.	AN	3	8
		ii	Find the minimized PLA of the following output Boolean function by a PLA minimizer f1 = (2,4,5,6,7,10,14,15): f2 = (4,5,7,11,15).	AN	3	5
14.	a		Design a Mealy machine that adds two 1-bit binary numbers along with a carry input, producing a sum and a carry output. Implement the design using a PLA.	CR	4	13
			Or			
	b	i	Discuss the process of state encoding for an FSM implemented in a PLD.	AP	4	6
		ii	Design a hazard free circuit for the following function f (ABCD) =A'BC' +A'B'C + CD'+AC.	AP	4	7
15.	a		Explain the different data types and operators used for modelling in verilog.	UN	5	13
			Or			
	b		How do you model a D flip-flop in verilog? Explain with suitable coding example.	UN	5	13

*PART – C (Marks 1*15 = 15)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
16.	a	Design a traffic light controller that cycles through Green (G), Yellow (Y), and Red (R) states based on a clock signal. The sequence is G -> Y -> R -> G. Implement the design using a PAL.	AP	4	15
		Or			
	b	Write a VHDL code to realize 4bit parallel adder using structural modelling and enumerate in flow chart.	AP	5	15